

DEC 30 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

U.S. Patent Application No.:	10/626,413)	
Filing Date:	July 24, 2003)	Group Art Unit: 2812
For:	Ferroelectric And High Dielectric)	Examiner: Ghyka, Alexander G.
	Constant Integrated Circuit Capacitors)	Docket No.: 13176.431C!US
	With Three-Dimensional Orientation)	Confirmation No.: 9869
	For High-Density Memories, And)	
	Method Of Making The Same)	
Applicants:	Paz de Araujo et al.)	

DECLARATION OF LARRY D. McMILLAN

I, Larry D. McMillan, hereby declare:

1. I am President and CEO of Symetrix Corporation at 5055 Mark Dabling Boulevard, Colorado Springs, Colorado, where I am involved in directing various research and business activities, which include integrated circuit manufacturing process development. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true.

2. I have worked for over 40 years as an integrated circuit process engineer. I have published more than one hundred papers and presentations on the subject of integrated circuit process engineering and have more than 75 issued US patents in the field. A copy of my curriculum vitae with a partial list of my papers and patents is attached hereto as Exhibit A.

3. I am an inventor in the above-identified patent application (hereinafter "the application") and Symetrix Corporation (Symetrix) is the assignee of the application.

4. I submit this Declaration to present to the Examiner, in an authenticated manner, facts concerning the relevance of the reference cited in the Office Action dated September 30, 2005 (hereinafter "the Office Action") and the patentability of the claims.

5. I have read the present claims of the application, the Office Action, and the reference cited by the Examiner, i.e., U.S. Patent No. 6,506,643, issued January 14, 2003, to Hsu et al. (hereinafter "Hsu et al.").

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6. The Office Action states that the claimed thicknesses of an 80 nm ferroelectric and a 200 nm capacitor laminate would be within the level of skill of one of ordinary skill in the art, for the benefit of storing more memory in less space. The portion of this statement that says that these thicknesses would be within the level of skill of one of ordinary skill in the art is incorrect.

7. Until the teachings of the present application, it was not possible for anyone, much less one of ordinary skill in the art, to make a three-dimensional capacitor with a ferroelectric film thickness not exceeding 80 nm and a capacitor laminate thickness not exceeding 200 nm as claimed in claim 1. As the Examiner has suggested, if this could have been done, Hsu et al. would have mentioned it, since it would make a more dense memory.

8. It has taken the inventors more than ten years to be able to make three-dimensional capacitors with film and capacitor laminate thicknesses this small.

9. A key aspect of being able to make capacitors with such small thicknesses was the low thermal budget deposition process, which is described in the present patent application. As described in the application, using this deposition method prevents damage that would lead to shorting of the extremely thin films.

10. The low thermal budget process was a true breakthrough, since prior to the invention of this process, those skilled in the art thought that better thin films could be made only by lowering the temperature.

11. However, as described on pages 16 and 17 of the present application, the low thermal budget process actually uses higher temperatures than prior art processes, but for a much shorter time.

12. The reduced heating time at elevated temperature of a low-thermal-budget technique in accordance with the invention reduces the formation of hillocks and other non-uniformities at the surfaces of deposited layers. The resulting enhanced smoothness improves interfacial contacts and inhibits electrical shorting. See page 37, lines 13–25, of the application.

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13. The low thermal budget also provides less heat to drive the oxygen used in the capacitor fabrication process to the transistor, thus preventing corruption of the transistor due to oxide production.

14. Another aspect of the invention that is helpful, but not necessary, in obtaining the thicknesses is the placing of the capacitor on a plug that gets it away from the transistor, which prevents the higher temperatures of the low thermal budget process from affecting the transistor and the back end reduction processes of the transistor from affecting the relatively delicate thin capacitor elements.

15. Another aspect of the invention that is helpful, but not necessary, is the use of only RTP, in contrast to the prior art furnace annealing, which allows the temperature to be ramped up and down quickly before it can deteriorate the electrodes and the transistor.

16. There are many other minor aspects described in the application that go together to allow us to have been the first to make workable 3-D capacitors so small.

17. Now that we have described how to make 3-D capacitors with such small dimensions, those skilled in the art will now know how to modify our processes to make small capacitors. For example, prior art heating processes could be used if the interlayer dielectric between the transistor and capacitor were made thicker so as to protect the transistor; or other designs could be used which, instead of using a thick interlayer dielectric, employed barrier layers that stopped oxygen and reduction gases from moving between the capacitor and transistor.

18. All of the above matters apply especially to 3-D capacitors, as opposed to 2-D capacitors because the thin layers spread over such large areas provide much more opportunity for a short or other problem to develop.

19. Since the inventors have shown for the first time how to make 3-D capacitors with extremely thin ferroelectric films and thin capacitor laminates, one skilled in the art may modify the processes and structures mentioned above to produce such capacitors without using one or more of the process and structural elements described in the application, but using the general principals taught in the application.

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20. Since these general principals were not obvious at the time of the invention, for the reasons given above, therefore, it is fair and equitable to grant applicants a patent on the current claims which describe a unique structure never before accomplished.

21. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

12-29-05

Date


Larry D. McMillan**BEST AVAILABLE COPY**

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Larry D. McMillan

CURRICULUM VITAE

EDUCATION

Ph.D. (Candidate) University of Colorado at Colorado Springs
M.S.E.E. Arizona State University, 1972
B.S. Aquinas College, 1965 (physics and mathematics)

Michigan Technological University, 1986-1993
Adjunct Professor

EXPERIENCE

1988-Present Symetrix Corporation
President and CEO
Corporate Management. Ferroelectric and other proprietary materials research and development, process and device development, program management and planning.

1984-1988 Ramtron Corporation
Vice President (R&D) and Corporate Founder
Member, Ramtron Board of Directors. Research and development of ferroelectric memory devices and integrated circuits. Primary investigations of phase three potassium nitrate and other ferroelectric materials.

1982-1984 Honeywell, Inc.
MOS Operations Manager
All MOS operations including wafer fabrication, maintenance, device engineering, process engineering, product engineering, test engineering, CAP/CAM, production testing and new process development. Member of Key Management Group (Corporate Level).

Manager, MOS Advanced Development
CAP/CAM development, CMOS process development, CCD TCL sensor process development, process transfers and long range planning activities. Developed and taught Operator and Technician Level IC Processing course (Honeywell Certificate Program).

MOS Process Engineering Manager
MOS production process engineering, maintenance, CCD process transfer from R&D to production, 3" to 4" wafer conversion, and advanced silicon gate MOS process development.

Larry D. McMillan

- 1980-1982 Stephenson Western, Inc.
Vice President
Engineering Consultant to the semiconductor industry. Computer modeling, fab design, UPDI water system design, process equipment selection, EPA regulations and hazardous chemical disposal. (Customer base included: Motorola, General Electric, Monolithic Memories, Fairchild, Signetics, Storage Technology, Intel and Mitel. (The firm was purchased by The Thomas Group.)
- 1979-1980 Storage Technology Corporation
Vice President and General Manager of Microtechnology Operations
Organized, staffed, designed and facilitated startup of semiconductor and thin film head and thin film media R&D and production facility.
- 1977-1979 National Cash Register (NCR) Corporation
Director of Engineering
All research, development and program management activities at the Colorado Springs NCR Integrated Circuit facility.
- 1976-1977 American Microsystems, Inc.
Manager, CMOS Process Engineering
All aspects of silicon gate CMOS process engineering, including process control and process development. VMOS and UMOS process development and transfer of NMOS process to Pocatello, Idaho facility. Developed and taught Operator and Technician Level Mathematics course.
- 1966-1976 Motorola, Inc.
Manager, Device Engineering (1975-1976)
Silicon gate NMOS fab device engineering and production process control. Established LPCVD silicon nitride and poly silicon as production processes in Austin, Texas facility.
- Staff Scientist, Advanced Product R & D Labs (1973-1975)
Process development of 4K and 16K NMOS RAMS. Multi-level metal MOS development, spin-on metallic oxide development, and LPCVD poly silicon and silicon nitride development.

Larry D. McMillan

CURRICULUM VITAE

Manager, Linear IC Wafer Engineering (1973-1970)

Expanded Mesa, Arizona linear IC manufacturing capability from 2,000-2" wafers to 14,000-3" wafers per week. Linear device engineering, specification control, process control, wafer process engineering, linear process development, HIREL pilot line and wafer test. Developed and taught Engineering Level Process Engineering Classes (Motorola Certificate Program).

Engineering Manager, Product Engineering Liaison (1969-1970)

Safeguard Missile Program (secret). Beam lead processing.

Engineer, Motorola Advanced Pilot Line (1967-1969)

Photoresist, metalization, product development.

Engineer, Motorola Training Program (1966-1967)

MOS process development, C-V analysis, multi-layer metal, Epi, materials research, packaging.

Larry D. McMillan

Publications and Presentations

Publications and Presentations

C.A. Paz de Araujo, **L. D. McMillan**, Z. Chen, Y. Shimada, Y. Kato, T. Otsuki, "Ferroelectric Linked Cell Device Physics", abstract presented at *The Proceedings of the 13th International Symposium on Integrated Ferroelectrics*, Colorado Springs, CO, March 2001.

Z. Chen, M. Lim, V. Joshi, Carlos A. Paz de Araujo, **L. D. McMillan**, "Advanced Simulation Tool For FeRam Design", abstract presented at *The Proceedings of the 13th International Symposium on Integrated Ferroelectrics*, Colorado Springs, CO, March 2001.

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Z. Chen, N. Solayappan, V. Joshi, K. Laetz, C.A. Paz de Araujo **L. D. McMillan**, "1K FeRam-Based Smart Card Application For Handspring Visor", abstract presented at *The Proceedings of the 13th International Symposium on Integrated Ferroelectrics*, Colorado Springs, CO, March 2001.

J. Karasawa, Y. Hamada, K. Ohashi, E. Natori, K. Oguchi, T. Shimoda, V. Joshi, **L. D. McMillan**, C. Paz de Araujo, "Effect of Process Condition on Microstructure of Thin SBT-Based Films", abstract presented at *The Proceedings of the 13th International Symposium on Integrated Ferroelectrics*, Colorado Springs, CO, March 2001.

S. Narayan, V. Joshi, J. Celinska, M. Lim, **L. D. McMillan**, C.A. Paz de Araujo, "Strontium Bismuth Tantalate Thin Films on IrO_x Bottom Electrodes For High Density FeRam Applications", abstract presented at *The Proceedings of the 13th International Symposium on Integrated Ferroelectrics*, Colorado Springs, CO, March 2001.

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J. Celinska, V. Joshi, S. Narayan, **L. D. McMillan** and C.A. Paz de Araujo, "Low Temperature Process for Strontium Bismuth Tantalate Thin Films", abstract presented at *The Proceedings of the 12th International Symposium on Integrated Ferroelectrics*, Aachen, Germany, March 2000.

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V. Joshi, N. Solyappan, J. Celinska, L.D. McMillan, C.A. Araujo, "A 650° C Process For Strontium Bismuth Tantalate thin films", abstract presented at The Proceedings of the 12th International Symposium on Integrated Ferroelectrics, Aachen, Germany, March 2000.

N. Solyappan, C. A. Paz de Araujo and **L. D. McMillan**, "Status of Advanced LSMCD for Y-1 Deposition," invited paper published in *Science Forum, Inc.*, Tokyo, 1999.

C. A. Paz de Araujo, N. Solyappan, **L. D. McMillan**, T. Otsuki and K. Arita, "Process Integration of Embedded FeRAMs", invited paper published in *Jour. ElectroCeramics, Special Issue*, 1999.

S. Narayan, V. Joshi, **L. D. McMillan** and C. Paz De Araujo, "Sub-100 nm SBT Films for Low Voltage and High Density FeRam Applications", *Proceedings of the 11th International Symposium on Integrated Ferroelectrics*, Colorado Springs, CO, Vol. 25, pp.509-517, March 1999.

M. Lim, J.W. Bacon, **L. D. McMillan** and C.A. Paz De Araujo, "SBT-Based Ferroelectric FET for Nonvolatile Non-Destructive Read Out (NDRO) Memory Applications", *Proceedings of the 11th International Symposium on Integrated Ferroelectrics*, Colorado Springs, CO, Vol. 27, pp. 1115-1124, March 1999.

N. Solyappan, V. Joshi, A. DeVilbiss, J. Bacon, J. Cuchiari, **L. D. McMillan** and C. A. Paz de Araujo, "Chemical Solution Deposition (CSD) and Characterization of Ferroelectric and Dielectric Thin Films", *Integrated Ferroelectrics*, Vol. 22, pp. 521-531, 1998

C. A. Paz de Araujo, T. Otsuki, J. Cuchiari and **L. D. McMillan**, "Microcontrollers with Ferroelectric Embedded Memory", presented at *IEEE 1998 International Nonvolatile Memory Technology Conference*, June 22-24, Albuquerque, NM, 1998.

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Y. Oishi, M. Azuma, S. Hayashi, **L. D. McMillan**, and C.A. Paz de Araujo, "Electrical Characteristics of Mn Doped Thin Film BST," abstract presented at *The Proceedings of the Seventh International Symposium on Integrated Ferroelectrics*, Colo. Spgs., CO, March 1995.

T. Sumi, N. Moriwaki, G. Nakane, T. Nakakuma, Y. Judai, Y. Uemoto, Y. Nagano, S. Hayashi, M. Azuma, T. Otsuki, G. Kano, J.D. Cuchiaro, M.C. Scott, **L. D. McMillan**, and C.A. Paz de Araujo, "256Kb Ferroelectric Nonvolatile Memory Technology for 1T/1C Cell with 100ns Read/Write Time at 3V," *Integrated Ferroelectrics*, Part 1, Vol. 6, pp. 1-13, 1995.

J.F. Scott, D. Galt, J.C. Price, J.A. Beale, R.H. Ono, C.A. Paz de Araujo, and **L. D. McMillan**, "A Model of Voltage-Dependent Dielectric Losses for Ferroelectric MMIC Devices," *Integrated Ferroelectrics*, Part 1, Vol. 6, pp. 189-203, 1995.

T. Otsuki, T. Sumi, E. Fujii, Y. Judai, Y. Shimada, N. Moriwaki, Y. Uemoto, M. Azuma, S. Hayashi, Y. Oishi, K. Arita, A. Inoue, T. Nagano, **L. D. McMillan**, and C.A. Paz de Araujo, "Ferroelectric Thin Film and Integration Technology, '95 MOCVD Workshop for Silicon Processing, Kyungju, Korea, pp. 224-226, 1995.

J.W. Gregory, J.D. Cuchiaro, C.A. Paz de Araujo, and **L. D. McMillan**, "The Effect of Thin Film Scaling on the Capacitance versus Voltage Characteristic of a Ferroelectric Memory Cell," *Integrated Ferroelectrics*, Part 1, Vol. 6, pp. 281-288, 1995.

Larry D. McMillan**Publications and Presentations**

Y. Shimada, Y. Nagano, E. Fujii, M. Azuma, Y. Uemoto, T. Sumi, Y. Judai, S. Hayashi, N. Moriwaki, J. Nakane, T. Otsuki, C.A. Paz de Araujo, and **L. D. McMillan**, "Integration Technology of Ferroelectrics and The Performance of the Integrated Ferroelectrics," *Proceedings of the Seventh International Symposium on Integrated Ferroelectrics, Colo. Spgs., CO, Vol. 11, Part 11, pp. 229-245, September 1995.*

C.A. Paz de Araujo, J.D. Cuchiaro, **L. D. McMillan**, M.C. Scott, and J.F. Scott, "Fatigue-Free Ferroelectric Capacitors with Platinum Electrodes," *Nature*, Vol. 374, pp. 627-629, April 1995.

L. D. McMillan, "Deposition of Barium Strontium Titanate and Strontium Titanate via Liquid Source Chemical Vapor Deposition", *Integrated Ferroelectrics*, Vol. 00, pp. 000-000, 1994.

J.F. Scott, C.A. Paz de Araujo, **L.D. McMillan**, "Ferroelectric Thin Films and Thin Film Devices", *Ferroelectric Ceramics*.

C.A. Paz de Araujo, B.M. Melnick, **L.D. McMillan**, "The Impact of Space Charge on the Measurement of the Dielectric Constant Using the C-V Method in Ferroelectric Memories", abstract.

M. Huffman and **L. D. McMillan**, "Liquid Source Misted Chemical Deposition: Technoloy Status and Recent Results", presented at the 2nd *Pacific Rim Conference on Ferroelectric Applications*, Melbourne, Australia, November, 1994.

L. D. McMillan, "Deposition of Barium Strontium Titanate and Strontium Titanate via Liquid Source Chemical Vapor Deposition", *Condensed Matter News*, Vol. 3, No. 4, 1994, p. IX, *Integrated Ferroelectrics*, Vol. 5, pp. 97-102, 1994.

T. Mihara, C.A. Paz de Araujo, J.D. Cuchiaro, H. Watanabe, and **L.D. McMillan**, "Feasibility for Memory Devices and Electrical Characterization of Newly Developed Fatigue Eliminated Ferroelectric Capacitors".

L. D. McMillan, M. Huffman, T.L. Roberts, M.C. Scott, and C.A. Paz de Araujo, "Deposition of $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$ and SrTiO_3 via Liquid Source CVD (LSCVD) for ULSI Drams," *Integrated Ferroelectrics*, Vol. 4, pp. 319-324, 1994.

J.F. Scott, M. Azuma, C.A. Paz de Araujo, **L. D. McMillan**, M.C. Scott, and T. Roberts, "Dielectric Breakdown in High- ϵ Films for ULSI DRAM's: II. Barium-Strontium Titanate Ceramics," *Integrated Ferroelectrics*, Vol. 4, pp. 61-84, 1994.

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B.M. Melnick, M.C. Scott, **L. D. McMillan**, and C.A. Paz de Araujo, "Characterization of a Spin-On 70/30 BST Process," abstract presented at *The 6th International Symposium on Integrated Ferroelectrics*, Monterey, CA, March 1994.

Larry D. McMillan**Publications and Presentations**

T. Ito, S. Hiraide, H. Yoshimori, H. Watanabe, T. Mihara, C.A. Paz de Araujo, M.C. Scott, and **L. D. McMillan**, "Characteristics of Ultra Thin Y-1 for a 1V Non-volatile Memory," abstract presented at *The 6th International Symposium on Integrated Ferroelectrics*, Monterey, CA, March 1994.

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PATENT # COUNTRY	DATE OF ISSUE	PATENT TITLE
45985 Singapore	03/30/99	Integrated Circuits Having Mixed Layered Superlattice Materials and Precursor Solutions For Use In A Process of Making The Same
53405 Singapore	09/21/99	Methods and Apparatus for Material Deposition Using Primer
56664 Singapore	11/16/99	Misted Precursor Deposition Apparatus and Method with Improved Mist Flow
56717 Singapore	03/14/97	Method and Apparatus for Fabricating Silicon Dioxide and Silicon Glass Layers in Integrated Circuits
DE 692 31 865 T 2 Germany	09/20/01	Layered Superlattice Material Applications
E201938 Austria	07/25/01	Layered Superlattice Material Applications
EP 0 616 723 Europe	06/20/01	Process For Fabricating Layered Superlattice Materials
EP 0 616 726 Europe	07/03/01	Layered Superlattice Material Applications
EP 0 665 814 Europe	01/15/97	Precursors and Processes for Making Metal Oxides
EP 0 665 981 Europe	03/20/02	Process For Fabricating Layered Superlattice Materials And Making Electronic Devices Including Same
EP 0 975 556 Europe	11/07/001	Method Of Forming Magnesium Oxide Films On Glass Substrate For Use In Plasma Display Panels
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NI 102545 Taiwan	08/19/99	Method and Apparatus for Fabricating Silicon Dioxide and Silicon Glass Layers in Integrated Circuits
NI 106205 Taiwan	12/30/99	Liquid Source Formation of Thin films Using Hexamethyl-Disilazane
NI 116293 Taiwan	01/10/01	Low Imprint Ferroelectric Material for Long Retention Memory and Method of Making the Same
NI 126 993 Taiwan	06/04/01	Misted Precursor Deposition Apparatus And Method With Improved Mist And Mist Flow
NI 130298 Taiwan	08/09/01	Ferroelectric Flat Panel Displays
NI 132591	09/13/01	Method Of Liquid Deposition By Selection Of Liquid Viscosity And

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202,532 South Korea	03/29/99	Methods of Apparatus for Materials Deposition
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5,487,032 USA	01/23/96	Method and Apparatus for Reduced Fatigue in Ferroelectric Memory Elements
5,508,954 USA	04/16/96	Method and Apparatus for Reduced Fatigue in Ferroelectric Memory
5,514,822 USA	05/07/96	Precursors and Processes for Making Metal Oxides
5,519,234 USA	05/21/96	Ferroelectric Dielectric Memory Cell Can Switch at Least Giga Cycles and has Low Fatigue - Has High Dielectric Constant and Low Leakage Current
5,523,964 USA	06/04/96	Ferroelectric Non-Volatile Memory Unit
5,540,772 USA	07/30/96	Misted Deposition Apparatus For Fabricating an Integrated Circuit

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USA		
5,541,870 USA	07/30/96	Ferroelectric Memory and Non-Volatile Memory Cell for Same
5,559,260 USA	09/24/96	Precursors and Processes for Making Metal Oxides
5,559,733 USA	09/24/96	Memory with Ferroelectric Capacitor Connectable to Transistor Gate
5,561,307 USA	10/01/96	Ferroelectric Integrated Circuit
5,612,082 USA	03/18/96	Process For Making Metal Oxides
5,614,252 USA	03/25/97	Method of Fabricating Barium Strontium Titanate
5,654,456 USA	08/05/97	Precursors and Processes for Making Metal Oxides
5,688,585 USA	11/18/97	Misted Deposition Method of Fabricating Layered Superlattice Materials
5,689,035 USA	12/16/97	ZNO Thin Film Varistors and Method of Making the Same
5,719,416 USA	02/17/98	Integrated Circuit with Layered Superlattice Material Compound
5,723,171 USA	03/03/98	Integrated Circuit Electrode Structure and Process for Fabricating Same
5,759,923 USA	06/02/98	Method and Apparatus for Fabricating Silicon Dioxide and Silicon Glass Layers in Integrated Circuits
5,784,310 USA	07/21/98	Low Inprint Ferroelectric Material for Long Retention Memory and Method of Making the Same
5,788,757 USA	08/04/98	Composition and Process Using Ester Solvents for Fabricating Metal Oxide Films and Electronic Devices Including the Same
5,792,592 USA	08/11/98	Photosensitive Liquid Precursor Solutions and Use Thereof in Making Thin Films
5,803,961 USA	09/08/98	Integrated Circuits having Mixed Layered Superlattice Materials and Precursor Solutions for Use in a Process of Making the Same
5,811,847 USA	09/22/98	PSZT for Integrated Circuit Applications
5,825,057	10/20/98	Process for Fabricating Layered Superlattice Materials and Making

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USA		Electronic Devices Including Same
5,840,110 USA	11/24/98	Integrated Circuits having Mixed Layered Superlattice Materials and Precursor Solutions for Use in a Process of Making Same
5,843,516 USA	12/01/98	Liquid Source Formation of Thin films Using Hexamethyl-Disilazane
5,846,597 USA	12/08/98	Liquid Source Formation of Thin films Using Hexamethyl-Disilazane
5,849,071 USA	12/15/98	Liquid Source Formation of Thin films Using Hexamethyl-Disilazane
5,871,853 USA	02/16/99	UV Radiation Process for Making Electronic Devices Having Low-Leakage-Current and Low-Polarization Fatigue
5,883,828 USA	03/16/99	Low Imprint Ferroelectric Material for Long Retention Memory and Method of Making the Same
5,888,583 USA	03/30/99	Misted Deposition Method of Fabricating Integrated Circuits
5,909,042 USA	06/01/99	Electrical Component Having Low-Leakage Current and Low Polarization Fatigue Made by UV Radiation Process
5,932,295 USA	08/03/99	Method and Apparatus for Misted Liquid Source Deposition of Thin Films with Increased Yield
5,942,376 USA	08/24/99	Shelf-Stable Liquid Metal Aryketone Alcoholate Solutions and Use Thereof in Photo Initiated Patterning of Thin Films
5,943,111 USA	08/24/99	Layered Superlattice Ferroelectric Liquid Crystal Display
5,955,754 USA	09/21/99	Integrated Circuits Having Mixed Layered Superlattice Materials and Precursor Solutions for Use in a Process of Making Same
5,962,085 USA	10/05/99	Misted Precursors Deposition Apparatus and Method with Improved Mist and Mist Flow
5,965,219 USA	10/12/99	Misted Deposition Method with Applied UV Radiation
5,966,318 USA	10/12/99	Nondestructive Readout Memory Utilizing Ferroelectric Capacitors Isolated From Bitlines by Buffer Amplifiers
5,972,428 USA	10/26/99	Methods and Apparatus for Material Deposition Using Primer
5,987,642 USA	12/07/99	Method and Apparatus For Misted Deposition of Integrated Circuit Quality Thin Films
6,017,579 USA	01/25/00	Method of Forming Magnesium Oxide Films on Glass Substrate for Use in Plasma Display Panels
6,022,669 USA	02/08/00	Method of Fabricating an Integrated Circuit Using Self-Patterned Thin Films
6,051,858	04/18/00	Ferroelectric/High Dielectric Constant Integrated Circuit and Method

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USA		of Fabricating Same.
6,056,994 USA	05/02/00	Liquid Deposition Methods of Fabricating Layered Superlattice
6,072,207	06/06/00	Process For Fabricating Layered Superlattice Materials And Making Electronic Devices Including Same
6,080,592 USA	06/27/00	Method of Making Layered Superlattice Materials for Ferroelectric, High Dielectric Constant, Integrated Circuit Applications
6,104,049 USA	08/15/00	Ferroelectric Memory With Ferroelectric Thin Film Having Thickness of 90 Nanometers or Less, and Method of Making Same
6,110,531 USA	08/29/00	Method and Apparatus for Preparing Integrated Circuit Thin Films by Chemical Vapor Deposition
6,116,184 USA	09/12/00	Method and Apparatus for Misted Liquid Source Deposition of Thin Film with Reduced Mist Particle Size
6,133,050 USA	10/17/00	UV Radiation Process for Making Electronic Devices Having Low-Leakage-Current and Low-Polarization Fatigue
6,143,063 USA	11/07/00	Misted Precursor Deposition Apparatus and Method with Improved Mist Flow
6,174,213 USA	01/16/01	Fluorescent Lamp and Method of Manufacturing Same
6,198,225 USA	03/06/01	Ferroelectric Flat Panel Displays
6,203,619 USA	03/20/01	Multiple Station Apparatus for Liquid Source Fabrication of Thin Films
6,258,733 USA	07/10/01	Method and Apparatus for Misted Liquid Source Deposition of Thin Film with Reduced Mist Particle Size
6,339,238 USA	01/15/02	Ferroelectric Field Effect Transistor, Memory Utilizing Same, And Memory of Operating Same
6,365,927 USA	04/02/02	Ferroelectric Integrated Circuit Having Hydrogen Barrier Layer
6,370,056 USA	04/09/02	Ferroelectric Memory And Method Of Operating Same
6,373,743 USA	04/16/02	Ferroelectric Memory And Method Of Operating Same
6,376,691 USA	04/23/02	Metal Organic Precursors For Transparent Metal Oxide Thin Films And Method Of Making Same
6,383,555 USA	05/07/02	Misted Precursor Deposition Apparatus And Method With Improved Mist And Mist Flow

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6,404,003 USA	06/11/02	Thin Film Capacitors On Silicon Germanium Substrate
6,413,883 USA	07/02/02	Method Of Liquid Deposition By Selection Of Liquid Viscosity And Other Precursor Properties
6,437,380 USA	08/20/02	Ferroelectric Device With Bismuth Tantalate Capping Layer And Method Of Making Same
6,441,414 USA	08/27/02	Ferroelectric Field Effect Transistor, Memory Utilizing Same, And Memory Of Operating Same
6,448,190 USA	09/10/02	Method And Apparatus For Fabrication Of Integrated Circuit By Selective Deposition Of Precursor Liquid
6,511,718 USA	01/28/03	Method And Apparatus For Fabrication Of Thin Films By Chemical Vapor Deposition
6,537,830 USA	03/25/03	Method Of Making Ferroelectric FET With Polycrystalline Crystallographically Oriented Ferroelectric Material
6,559,469 USA	05/06/03	Ferroelectric And High Dielectric Constant Transistors
6,582,972 USA	06/24/03	Low Temperature Oxidizing Method Of Making A Layered Superlattice Material
98909128.5-2111	03/12/98	Method of Forming Magnesium Oxide Films on Glass Substrate for Use in Plasma Display Panels